PAUL SCHERRER INSTITUT

Direct-Sampling CW Digital Low-Level RF for 50 MHz Cyclotrons at PSI

LLRF 2019

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Abstract

In the long-term project frame of the HIPA (High Intensity Proton Accelerator) RF systems, the replacement of analog LLRF from the decades 1980's/90's with a digital system is on-going.

All functionality of the old existing electronic circuits were converted into the new digital LLRF system. The key feature is the direct sampling RF receiver which provides RF amplitude and phase information at various sampling rates and resolutions for the internal processing resources such as FPGA or CPU.

Due to the high integration compared to the existing analog LLRF, which had splitted RF signals for each individual function, now a single instance of an RF receiver channel per RF signal can serve multiple functions in the digital domain. These functions such as fast RF field feedback control, cavity tuning feedback control, RF system startup or RF system fault detection and logging are presented with details on requirements, implementation, performance and limitations.

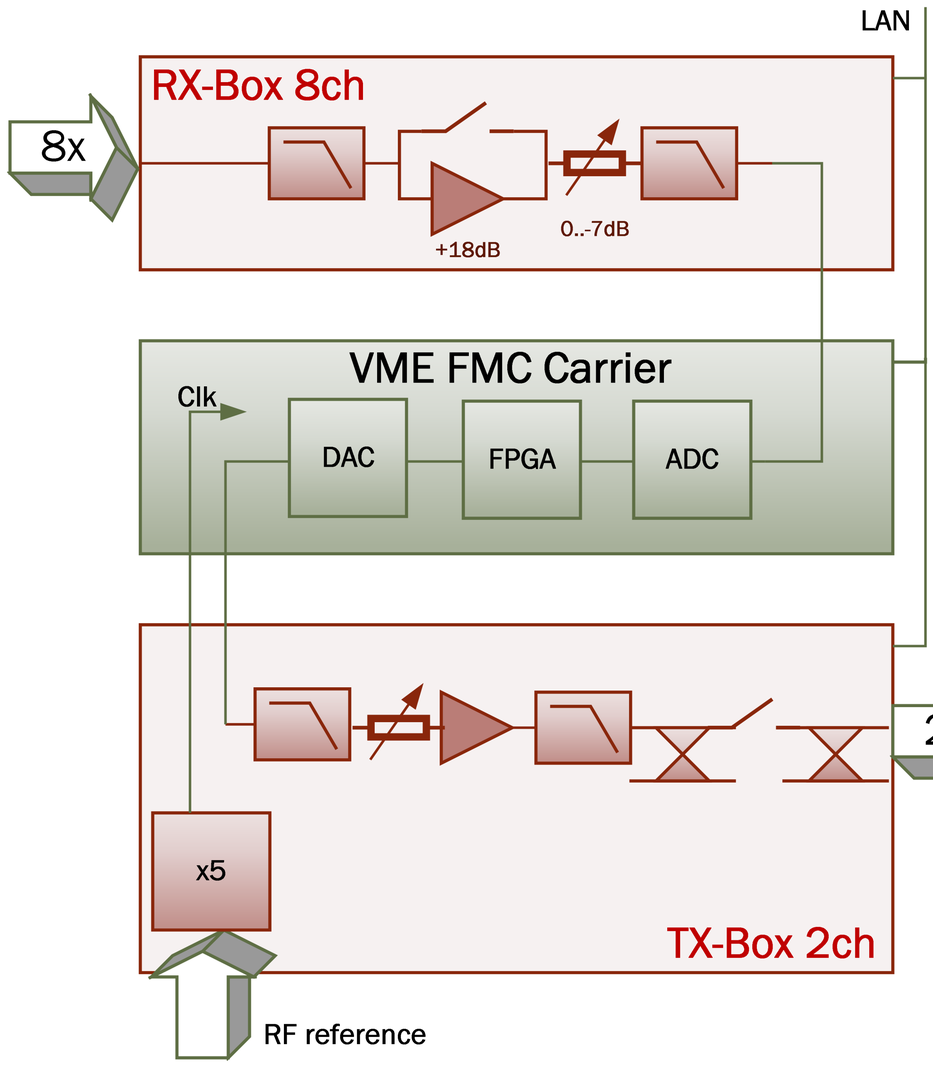


Figure 1: Block diagram of 50 MHz CW LLRF, shown 8 DAQ channel version

Figure 2: RX-Box prototype (front and rear view)

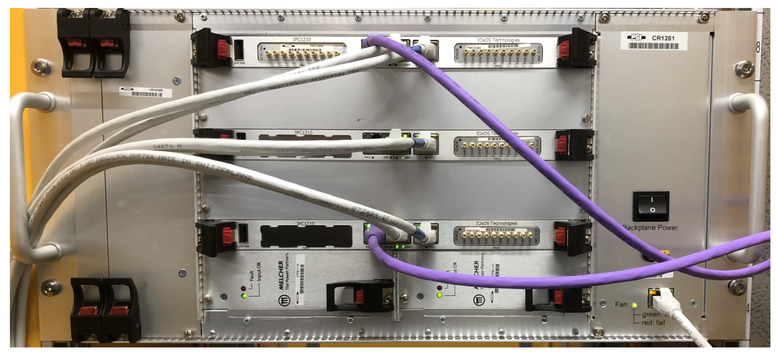


Figure 3: VME Crate for 24 channel LLRF with 3 FMC carrier boards

Figure 4: TX-Box prototype (front and rear view)

LLRF signal processing

The statistics processing shall deliver data set (i.e. amplitude and phase) from all eight ADC channels at lowered sampling rate fixed at 50.6 kHz to real time application software. The real time software will process statistics at 10 Hz (i.e. 5060 Samples). For purpose of RF fault evens analyzes, post-mortem amplitude waveforms are available with 25 MSps. rate for all channels.

ADC input data sampling rate is set by design, at 5 x Cavity RF (5 x 50.63282 MHz ~= 253 MHz).

Due to the high decimation rate required (500), CIC and FIR filters will be used in order to realize the digital down conversion (DDC). The frequency band of interest is in base band up to approx. 20 kHz. The following figure shows the pseudo-RTL architecture. It's important to remark that data enter parallel and are during first processing stage time-division multiplexed for a maximal resource optimization.

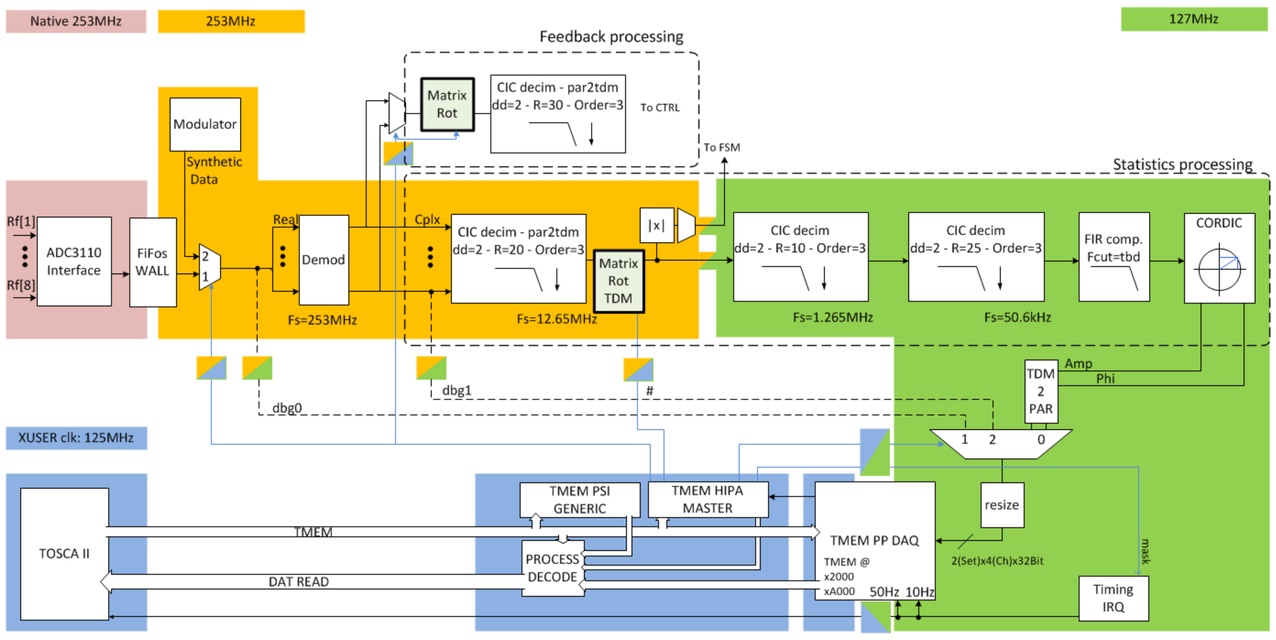
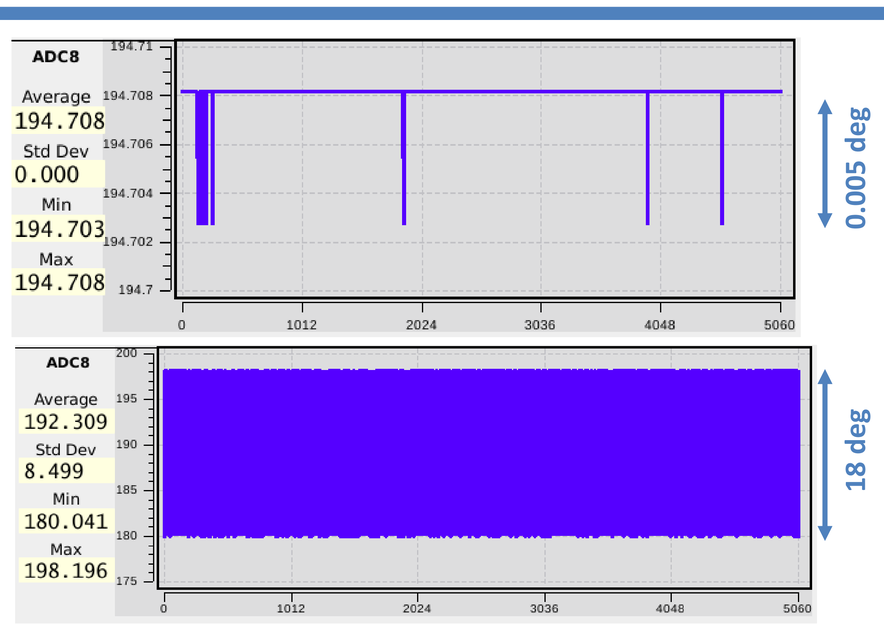


Figure 5: Block diagram 50 MHz LLRF Data Acquisition (DAQ) processing in FPGA.



LLRF signal processing input level:

0 dBFS

-80 dBFS

Figure 6: LLRF DAQ waveforms for phase of 50 MHz reference signal at -20 and -100 dBFS input level, sampled at 50.6 ksps

LLRF A/Ph feedback processing

The feedback controllers for the amplitude and phase are implemented as two independent controllers in the polar coordinate system. This allows to enable and disable the two loops independent from each other. The controller sample rate is 8.4 MSps. and the clock domain is 127 MHz. As input of the controllers a multiplexer on the ADC / LLRF DAQ channel is used to select either cavity input or cavity pickup signal.

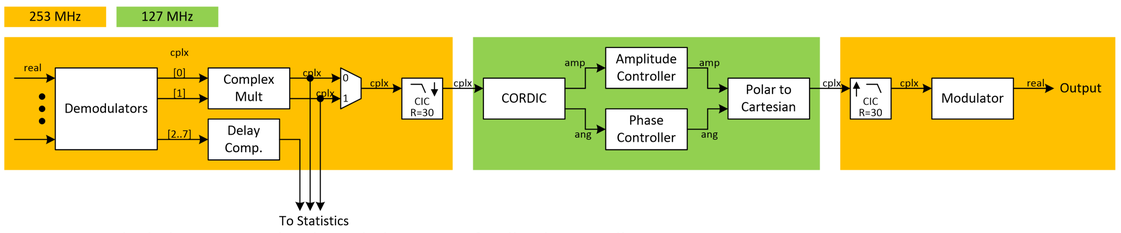


Figure 7: Block diagram amplitude and phase LLRF feedback controllers

RF startup procedure

For the reliable and safe start-up of the RF power amplifiers into the narrowband cavity, a special RF start-up procedure is required to implement in the LLRF system.

Cavity characteristics:

- 50 MHz, Q_0 = 25 k, BW = 2 kHz

After applied a minimum RF level, the LLRF cavity tuning loop starts to tune with mechanical plungers. It is using the cavity input and cavity probe phase measurements from the LLRF DAQ.
In parallel, RF pulsing starts with short ~200µs long high power RF pulses. If the cavity input reflected amplitude at RF pulse end is below a certain threshold, then the cavity is tuned and CW RF operation at nominal power is allowed.

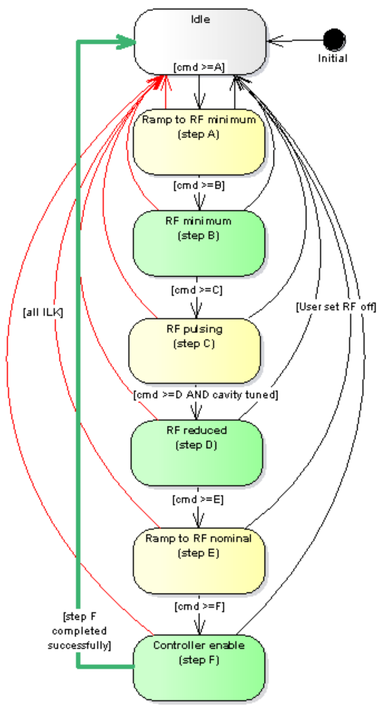


Figure 8: Start-up Sequencer FSM

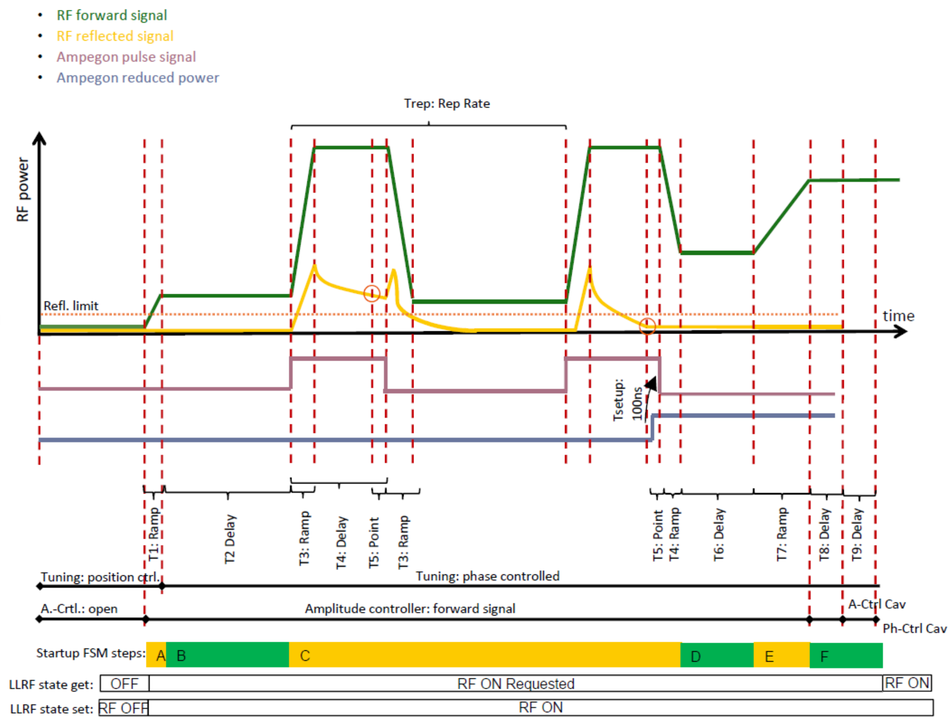


Figure 9: Startup Procedure Timing Waveform Diagram

Conclusion / Outlook

The implementation of the new 50 MHz LLRF system for HIPA is in the state of lab characterization and initial tests at dedicated high power cavity test stand. The LLRF analog frontend hardware is ready in a prototype version. The digital hardware is the same hardware as already used for the SwissFEL LLLRF (IF there is 40 MHz). The firmware / software implementation is on-going.
Critical points are the high dynamic range of ~100 dB for the phase measurements for the purpose of the cavity tuning. Simulation and tests shall be show where the FPGA fixed point signal processing chain (e.g. bit width) can be extended to improve the readout resolution in high and low signal case and how analog pre-amplifiers can be used.
The integration tests of the RF startup procedure have to prove that all exceptions are handled in a reliable way.

Revision 2, Roger Kalt roger.kalt@psi.ch , Matthias Stoll matthias.stoll@psi.ch 26.09.2019, presented at LLRF Workshop 2019 (LLRF2019, arXiv:1909.06754)